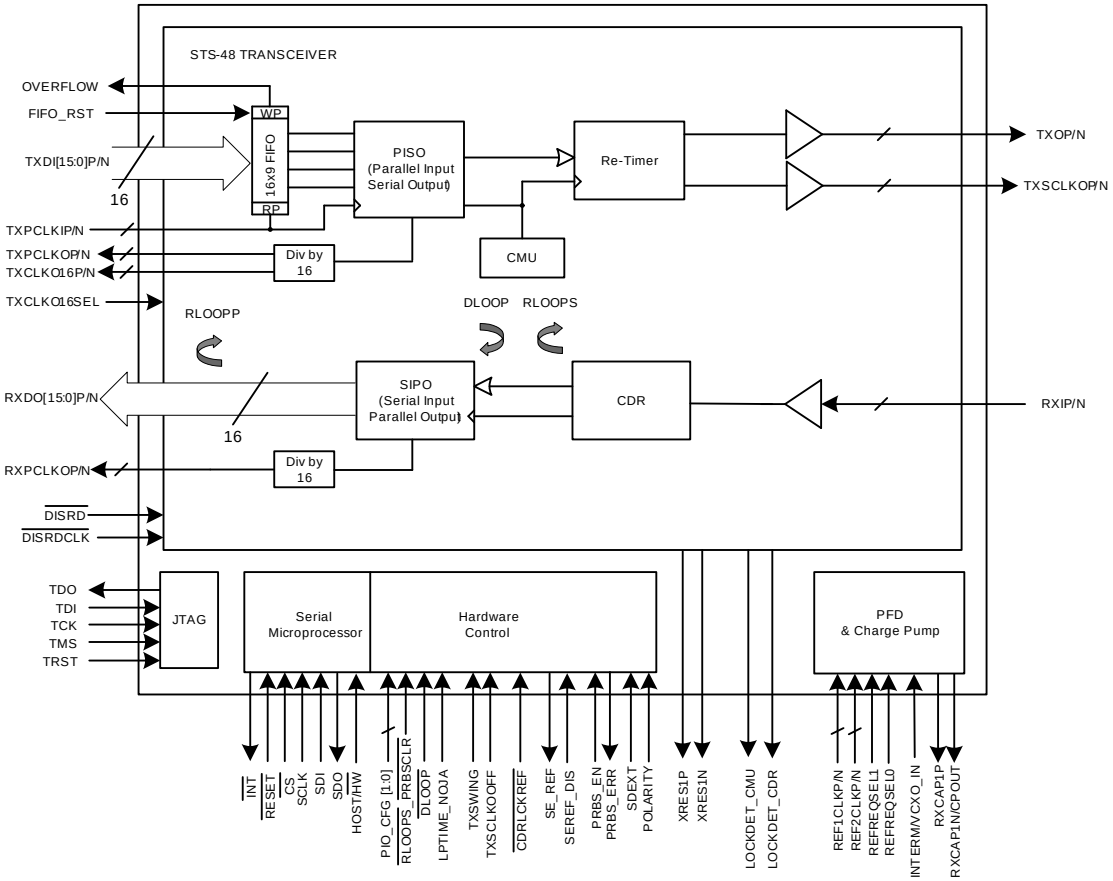
2.488/2.667 GBPS STS-48/STM-16 SONET/SDH XRT91L82 Transceiver Evaluation Board User Manual

Figure 1.0 XRT91L82 Block Diagram



1.0 OVERVIEW

This is evaluation board manual is intended to help the user become familiarized to operate the XRT91L82 Evaluation Demo Board and run traffic with minimum effort.

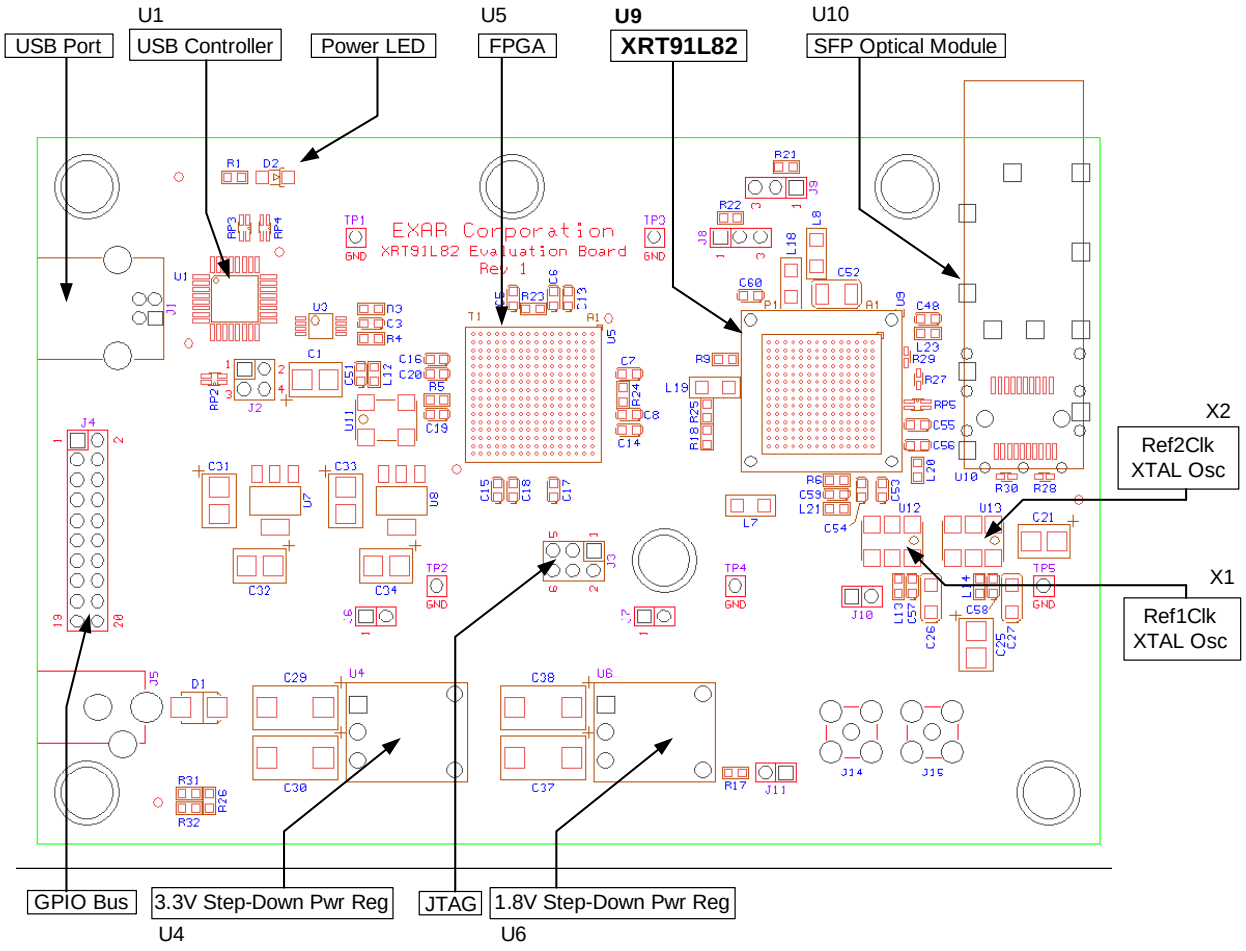
Requirements:

1. XRT91L82 Evaluation Demo board
2. OC-48/STM-16 generator/analyzer test equipment
3. A Windows PC with USB port & USB cable for power supply and GUI interface
4. XRT91L82 supplied USB drivers and GUI to be installed on the PC (using Win98SE, 2000, or XP)
5. XRT91L82 data sheet (rev P1.0.7 or newer)

2.0 Evaluation Board Architecture

XRT91L82 Evaluation Board provides a simple and efficient way to quickly evaluation functionality and performance of the XRT91L82 SONET/SDH STS-48/STM-16 Transceiver.

Figure 2.0 XRT91L82 Evaluation Board Revision 1



Evaluation board consists of XRT91L82 device (U9) connected to a Small Form Factor Pluggable (SFP) optical module (U10). The XRT91L82 hardware control pins are interfaced to an FPGA, where the state of the FPGA pins is controllable by a Graphical User Interface running on a Personal Computer connected to the Evaluation Board via the Universal Serial Bus (USB) interface.

A 155.52 MHz differential (LVPECL) crystal oscillator (U12) provides the reference clock needed by the XRT91L82 **P**hase-**L**ocked **L**oop (PLL) components. Evaluation board power is provided by the personal computer through the USB port.

The 5V supplies power to two step down switching power regulator modules (U4 & U6) which provides 3.3V and the 1.8V power required by the XRT91L82 device.

2.1 FUNCTIONALITY AND CONTROL

The FPGA controls all of the function of the XRT91L82 device. All access to XRT91L82 Hardware Control pins are defined through the use of the Exar supplied XRT91L82 GUI. The XRT91L82 GUI allows switching of Hardware Control pins to either "high" state or "low" state. Switching to Host Mode permits the Exar supplied XRT91L82 GUI to control and access the XRT91L82 silicon through the 4-bit serial processor interface thereby allowing use of additional features such as performance monitoring and interrupt polling.

2.2 XRT91L82 REFERENCE CLOCK

All XRT91L82 boards are shipped with a standard 155.52 MHz LVPECL differential reference clock oscillator. The 155.52 MHz oscillator is connected to the XRT91L82's reference clock inputs REF1CLKP/N. The user must choose the appropriate reference clock frequency setting to properly operate the XRT91L82 based upon the state of REFREQSEL1 pin D12 and REFREQSEL0 pin E12 in Hardware Mode of operation or the logic levels of REFREQSEL1, REFREQSEL0, and ALTFREQSEL bit in the XRT91L82 software register in Host Mode of operation.

2.3 FPGA PARALLEL BUS INTERFACE FEATURES

OC-48/STM-16 optical signal is received by the optical module and converted to Differential CML electrical signal before being interfaced to the XRT91L82. The XRT91L82 then recovers the clock and data and converts the serial data to SONET/SDH 16-bit wide parallel data and outputs both the data and the recovered divide-by-sixteen clock that is synchronous to the parallel data. The FPGA performs the task of the terminal end unit and allows a system level FPGA Remote Loopback function, where the received data from the XRT91L82 is looped back within the FPGA and sent to the transmit input interface of the XRT91L82.

Note:
This is system level loopback is significantly different from the XRT91L82 device's diagnostic Serial Remote Loopback. Serial Remote Loopback occurs internally within the XRT91L82 and received serial data is looped back to the transmitter before **ser**ial-**des**erializer (SERDES) conversion. Serial Remote Loopback is meant to be used for diagnostics.

In addition, the XRT91L82 also contains an internal $2^{23} - 1$ PRBS pattern generator and PRBS data integrity checker. A status LED indicator called **Pattern Error** indicates if there is a current loss of PRBS sequence or a momentary loss of PRBS sequence.

2.4 EVALUATION BOARD LIMITATIONS

1. Only the LVDS interface is supported on the Transmit and Receive Parallel bus.
2. Internal 100 ohms terminations must be used.
3. Loop timing must be implemented when using Ext (FPGA) Remote Loopback.

Limitation 1 & 2: Due to large number of differential pair connections between the FPGA and the XRT91L82 and additional line termination components required by the PECL interface only the LVDS option was implemented on the evaluation board. For LVDS option the internal 100 Ohm terminations on the XRT91L82 and FPGA are used.

Limitation 3: Whenever **Ext (FPGA) Remote Loop back** is used, **Loop timing** must be implemented. This guarantees that transmit timing is synchronous to the signal source timing.

3.0 USB DRIVER AND GRAPHICAL USER INTERFACE INSTALLATION

This section details the installation of the software GUI provided as part of the evaluation process. It includes the following topics:

3.1 Installing the Exar USB Driver
3.2 Installing the Evaluation Software

3.1 INSTALLING THE EXAR USB DRIVER

In order to operate the XRT91L82 GUI with the XRT91L82 Evaluation board, it is necessary to install the Exar USB drivers. Upon plugging the evaluation board into the computer, the system should recognize a new device and prompt for a driver. A window should appear similar to the one below.

Figure 3.0 Add New Hardware

Note:
Included in the driver zip package are two files: “exarusb.inf” and “exarusb.sys.” Upon first connecting the board to your computer, you may be prompted to install the Exar USB drivers. To install the drivers, follow the prompts and manually select the “exarusb.inf” file from the included driver zip file.

The drivers are included in the Exar CD in the folder labeled Drivers. To install from the CD, select **Display a lists of all the drivers in a specific location, so you can select the driver you want**.

Figure 3.1 Select Display Available Drivers and then Next

Figure 3.2 Select "Other detected devices" and then Next

Figure 3.3 Select Have Disk

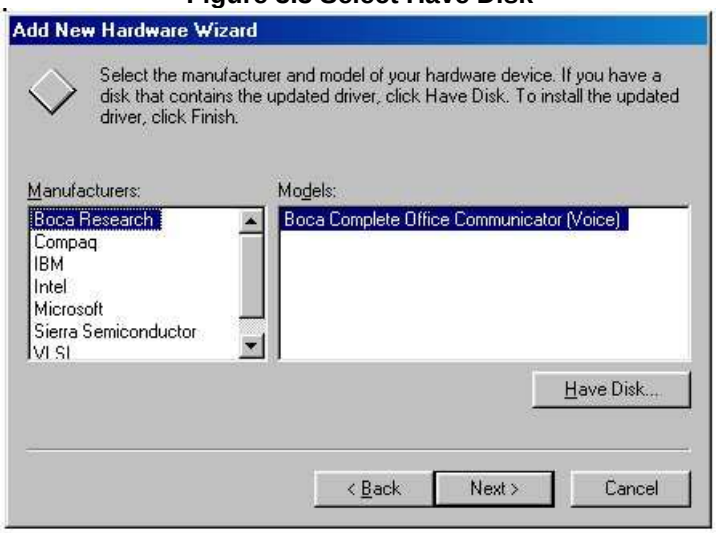
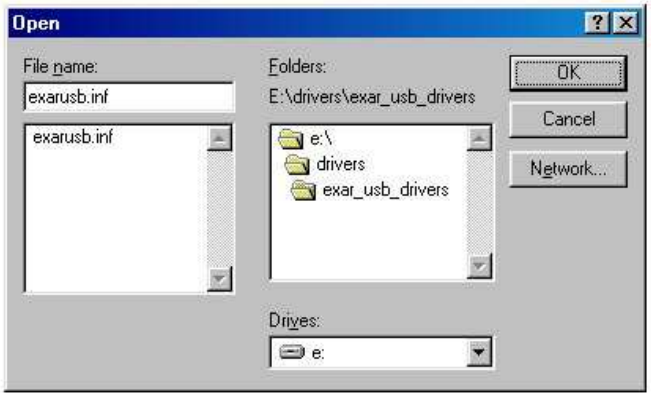
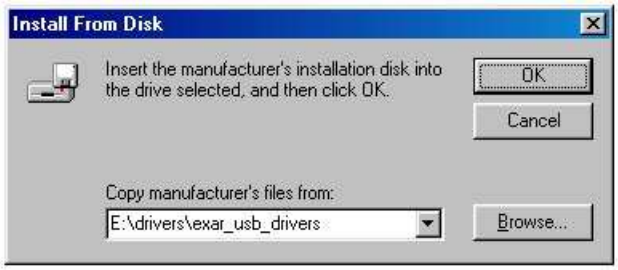


Figure 3.4 Find the location of the drivers located on the CD



The following window will appear confirming the location of the driver.
Select OK

Figure 3.5 Install From Disk



The driver will appear in the Have Disk window and should be selected. Press Next to install the driver.

Figure 3.6 Driver Select

Now that the system has found the appropriate drivers, select Next to install the Exar driver.

Figure 3.7 Install Driver

The driver is now installed in the operating system software and the computer is now ready to run the Exar Evaluation GUI.

Figure 3.8 Installation Successful

4.0 INSTALLING THE XRT91L82 EVALUATION GUI

To install the XRT91L82 GUI, double click on the installation file enclosed in the CD, as part of the evaluation package. This will place the relevant GUI files in an Exar created folder along with the necessary FPGA file. Since the XRT91L82 may be operated in hardware mode, the GUI will load the FPGA file necessary to drive the input pins and control the XRT91L82 device. This is automatically done when **Test->Start Test** is selected.

4.1 STARTING THE EVALUATION SOFTWARE

The evaluation software allows the user to do the following:

- Configure the XRT91L82 for proper operation
- Poll current alarm status.
- Enable/Disable XRT91L82 features with the click of a button

Once the XRT91L82 GUI is installed, it can be found through the **Start Menu->Exar->XRT91L82 Evaluation**. Once selected, it will open up the application. To begin the GUI and device evaluation, select **Evaluation** from the menu bar and then **Start Evaluation**. This will bring up the dialog box.

Figure 4.0 Start Test

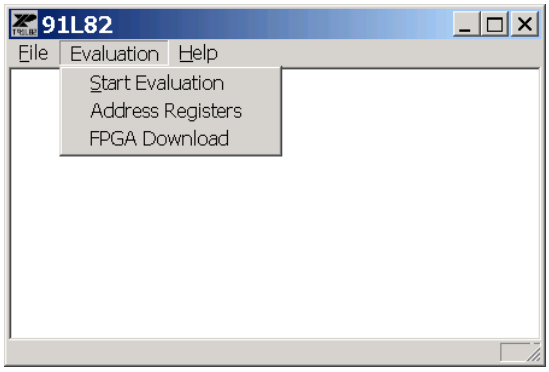
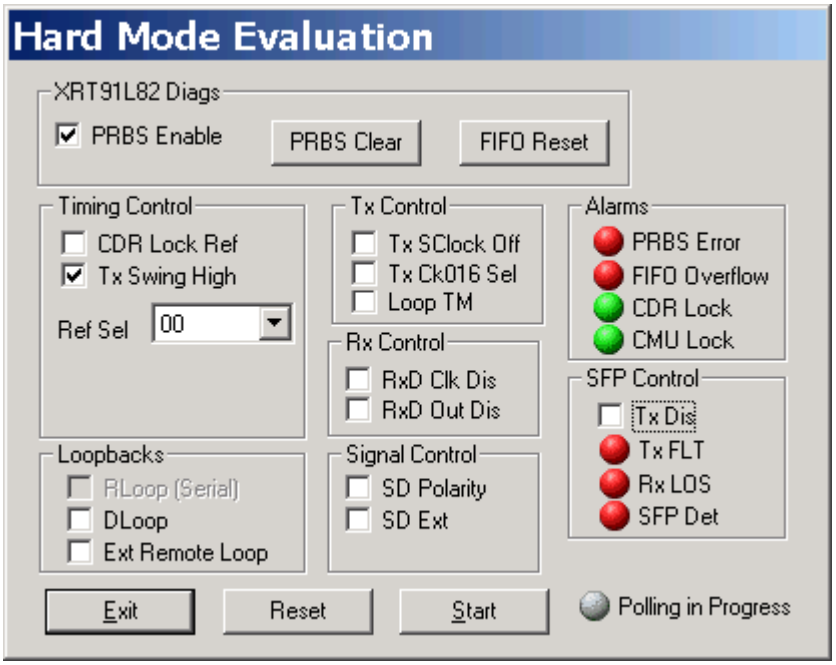


Figure 4.1 Main Hardware Mode GUI Window



Make sure the following are correct:

1. Connect the power supply to the board (all power is derived on board from the 3.3 volt supply.
2. Connect the PC to the board with the USB port cable.
3. Connect an optical cable to the SFM module from a signal source.
4. Power up the system and verify that the PC to XRT91L82 communications are working.

4.2 HARDWARE MODE GUI BLOCK DESCRIPTION

Tx/Rx Control:
This register allows the user to control the input/output signal.

Alarm Status:
This register reflects the alarms that occur.

Timing Control:
This register allows the user to control the clock timing.

Test Control:
This register allows the user to control the Loopbacks and PRBS pattern generation.

4.3 BUTTON DESCRIPTIONS

Start:
This button will start the polling test of the XRT91L82.

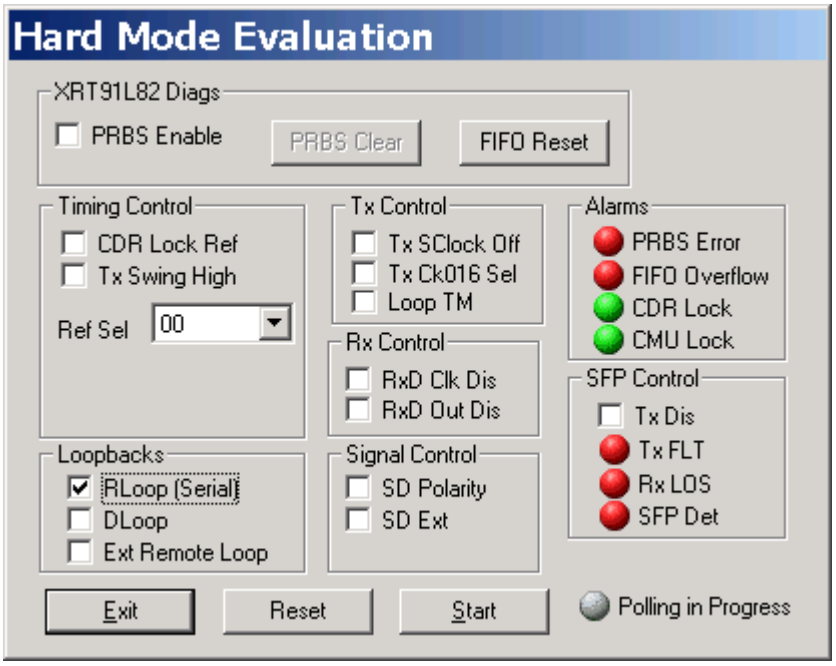
Stop:
This button will stop the polling test of the XRT91L82.

Reset:
Resets the software registers of the XRT91L82.

4.4 REMOTE SERIAL LOOPBACK USING GUI

Set the XRT91L82 into the remote (serial) loopback mode and verify that the board is receiving and transmitting data. Figure 4.2 indicates the selection.

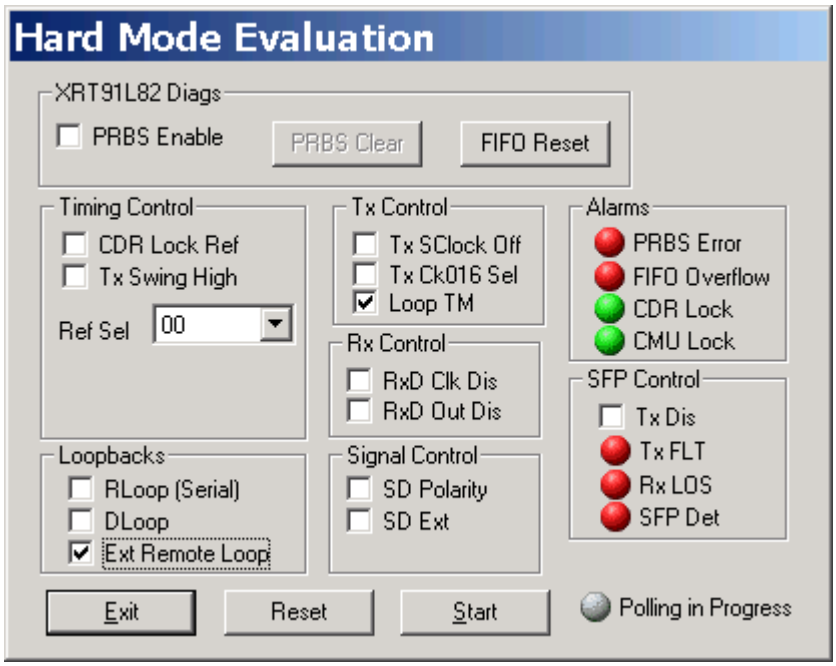
Figure 4.2 GUI with Remote Serial Loopback Enabled



4.6 EXTERNAL LOOPBACK USING GUI

Switch to external loopback (disable Remote loopback mode) and verify that the data flows out of the receive section, through the cables from the RXDOn pins to the TXDIn pins, and back out the transmit section to the test equipment. See Figure 4.3.

Figure 4.3 External Loopback mode

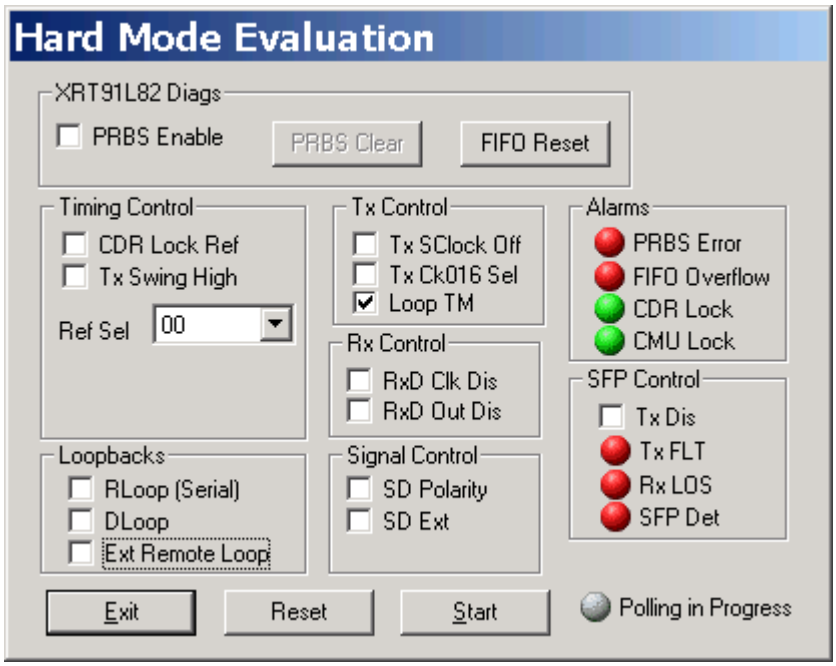


Note: After starting test, the “FIFO Reset” should be activated (and deactivated) to Flush the FIFO.

4.7 TX/RX RUNNING INDEPENDENT USING GUI

No loopback mode (Tx and Rx running independent) is shown in Figure 4.4.

Figure 4.4 TX & RX w/ REFCLK @ 155.52 MHz



Note: After starting test, the “FIFO Reset” should be activated (and deactivated) to Flush the FIFO.

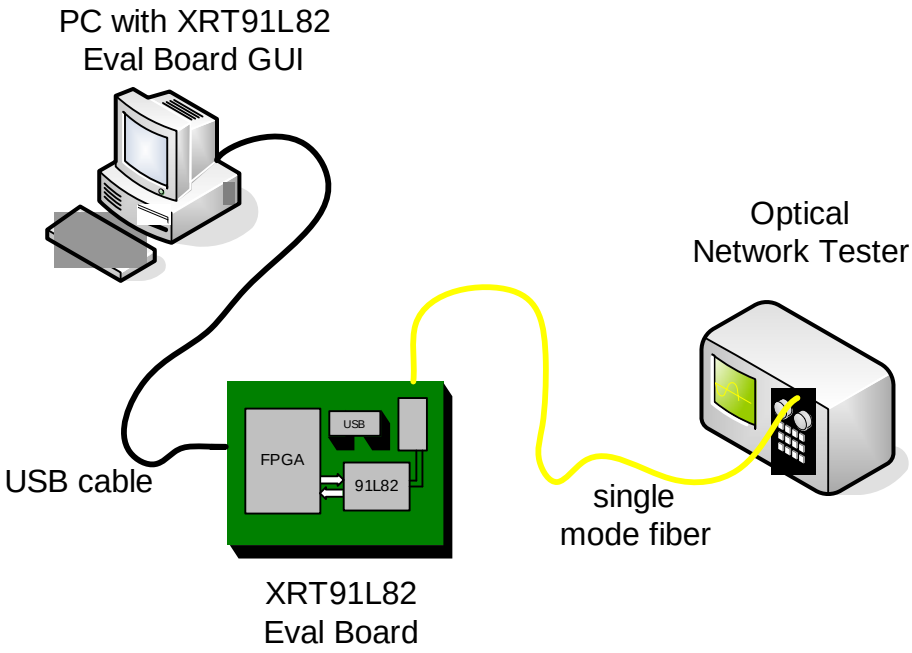
5.0 SETTING UP THE XRT91L82 EVALUATION BOARD FOR SONET/SDH TESTING IN HARDWARE MODE

The XRT91L82 Evaluation Board can be used to test the STS-48/STM-16 high-speed serial interface and the 155.52 Mbps low-speed 16-bit parallel bus interface. High-speed OC-48/STM-16 serial data is injected at the SFP optical module interface after which it is converted to STS-48/STM-16 electrical signal. The XRT91L82 will perform clock and data recovery and present the 155.52 Mbps low-speed 16-bit parallel data to the FPGA. The following sections cover the hardware mode test setup.

To successfully perform this test, you must have the following equipment:

- XRT91L82 Evaluation Board
- A PC based on Windows 98SE, NT4.0, 2000, or XP operating system platform
- An optical OC-48/STM-16 SONET/SDH test equipment
- An optical attenuator if necessary

Figure 5.0 Hardware Mode SONET/SDH Transceiver Test Setup



Use the following steps in configuring the XRT91L82 Evaluation Board.

1. Install Exar supplied USB drivers and XRT91L82 GUI on the PC.
2. Connect the Exar supplied standard USB cable to the PC.
3. Connect PC USB cable to the USB Port on the board. Verify power supply on the board by checking Power LED.
4. Connect optical cable to from the OC-48/STM-16 SFP module to the Optical Network Test Equipment. Verify optical signal strength and attached an optical attenuator to the receiver end of the test equipment if necessary.
5. Launch XRT91L82 GUI Application.
6. Configure the XRT91L82 for proper data rate and operation.

6.0 EXAMPLE APPLICATIONS

The following example applications are provided in this manual:

6.1 LOOPBACK OPERATIONS

Loopback operations generally fall under 2 different categories and are referenced with respect to the device. Remote loopback and Local Loopback are both available on the XRT91L82 device. Remote Loopback indicates that remote equipment (test equipment) signal is routed back to the equipment. Hence, all types of remote loopback routes received signal back to the transmit side. Local loopback indicates that link layer or terminal equipment signal (hence, local signal) is routed back to the link layer or terminal equipment. This means locally transmitted signal is routed back to the receiver.

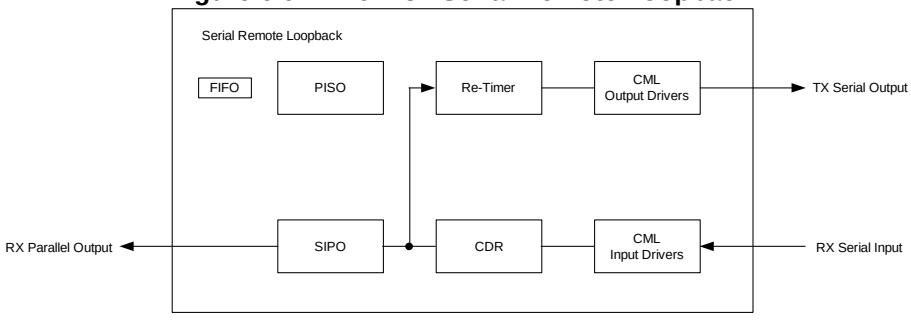
There are a total of two types of loopback operations available in Hardware Mode on the XRT91L82. The loopbacks are remote equipment loopback and one is a local terminal equipment loopback:

- Remote Serial Loopback
- Local Digital Loopback

6.1.1 Serial Remote Loopback

To quickly diagnose line integrity back to remote or test equipment, a serial remote loopback can be invoked.

Figure 6.0 XRT91L82 Serial Remote Loopback



Configuring for Remote Serial Loopback Operation

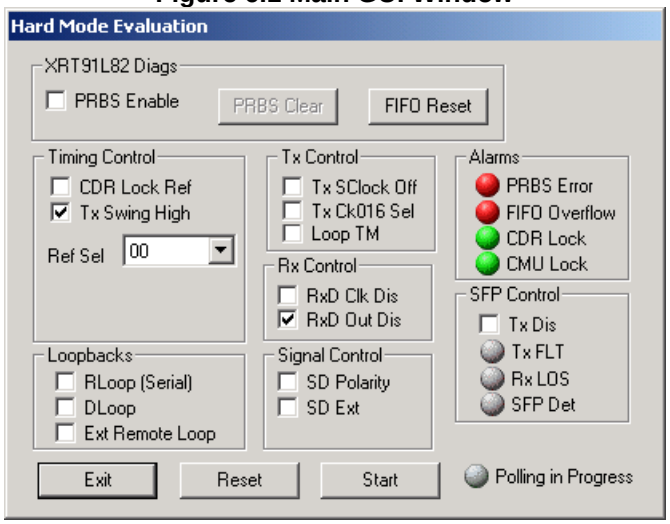
Step 1. With the Exar USB drivers and the XRT91L82 GUI installed, connect the USB cable to both the PC and the XRT91L82 Evaluation Board. Verify power supply on the board by checking Power LED.

Step 2. Connect the optical cable from the SFP module on the Evaluation Board to the OC-48/STM-16 Optical Network Test Equipment. This cable is included in the XRT91L82 evaluation kit. Verify optical signal strength and attached an optical attenuator to the receiver end of the test equipment if necessary.

Step 3. Launch the XRT91L82 application GUI. See section 4.1, "Starting the Evaluation Software."

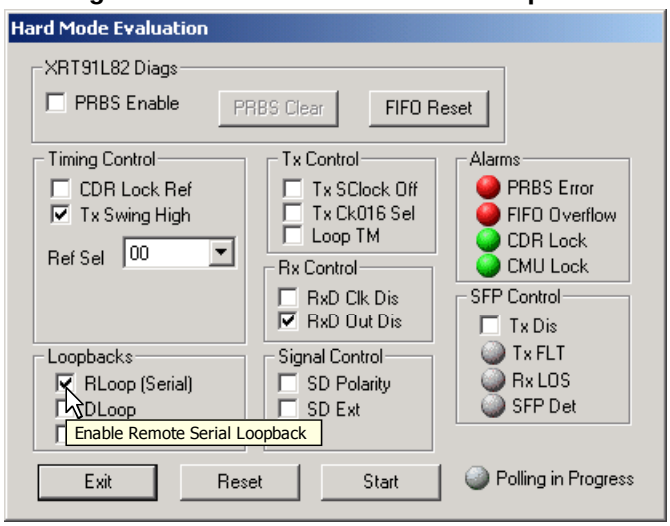
Step 4. Once the application GUI **Start Test** is running, you should see a similar window below with the XRT91L82 default settings. You are now ready to execute the XRT91L82's features and functions.

Figure 6.1 Main GUI Window



Step 5. Enable the Remote Serial Loopback by checking the on the "**RLoop (Serial)**" box.

Figure 6.2 Enable Serial Remote Loopback

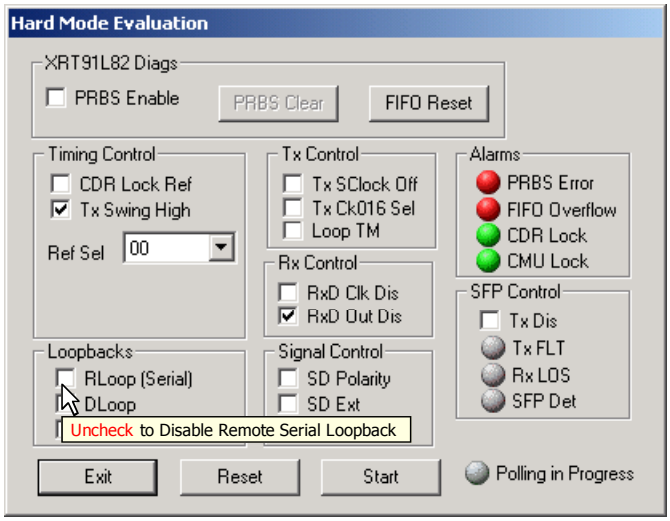


Step 6. Check test equipment for valid pattern synchronization.

Note: If the test equipment receiver reports a Loss of Signal, it is likely that the optical cable is not properly oriented. Switch the transmit and receive cables on the test equipment and verify data integrity.

Step 9. (OPTIONAL) To disable Remote Serial Loopback, uncheck the "**RLoop (Serial)**" box.

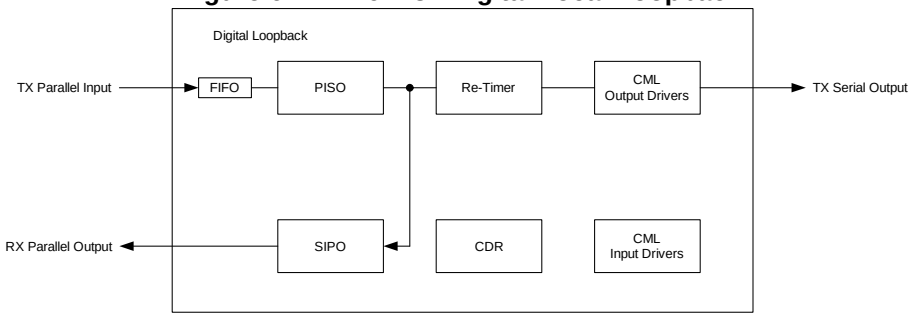
Figure 6.3 Disable Serial Remote Loopback



6.1.2 PRBS Pattern Synch Test using Digital Local Loopback

This loopback needs to be invoked whenever local diagnostic is desired as such when the PRBS generator and analyzer are used. Local transmit data is looped-back at the parallel input to serial output converter.

Figure 6.4 XRT91L82 Digital Local Loopback

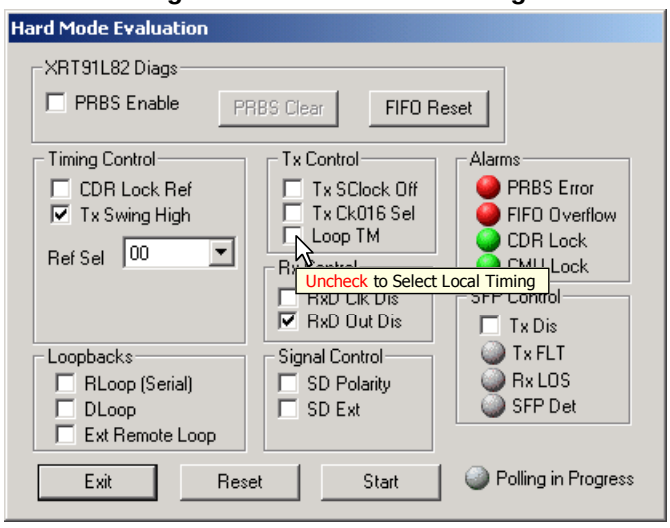


Configuring for 2^{23} – 1 PRBS pattern test using Digital Local Loopback Operation

Step 1. Proceed with the same steps as Step 1 through Step 4 for Remote Serial Loopback Operation in configuring the XRT91L82 board.

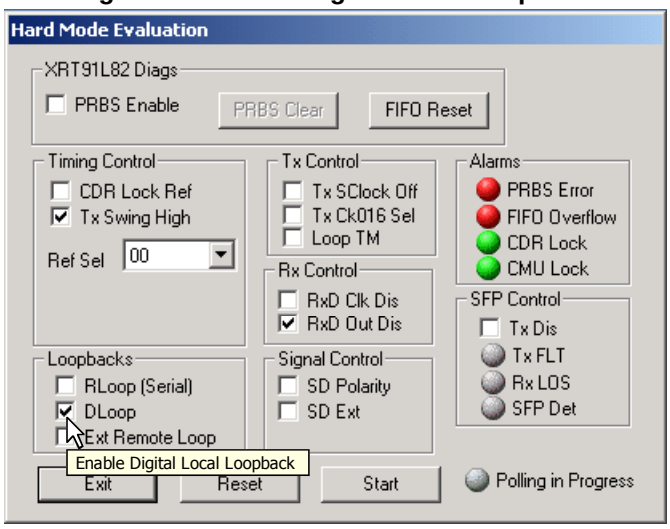
Step 2. Select **Local Timing** mode for the XRT91L82 transmit timing.

Figure 6.5 Select Local Timing



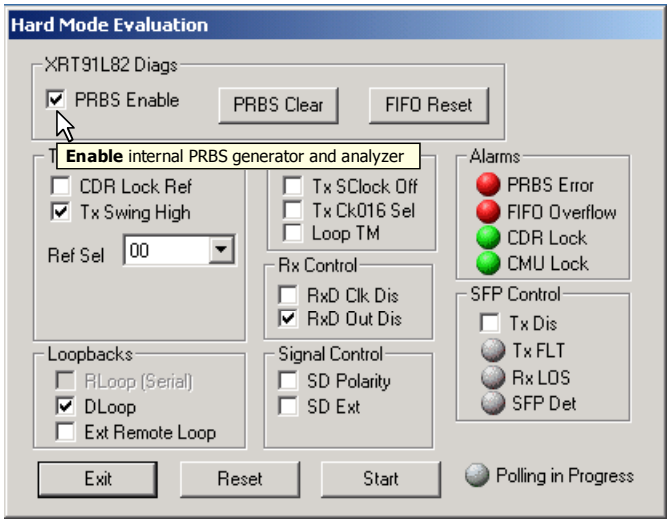
Step 5. Enable the Digital Local Loopback by checking the "**DLoop**" box in **Loopbacks** section.

Figure 6.6 Enable Digital Local Loopback



Step 6. To enable the 2^{23} -1 PRBS pattern generator and analyzer block within the XRT91L82, select the "**PRBS Enable**" box from the pattern selection menu. Remote Serial Loopback will not be available once the pattern generator and analyzer is enabled.

Figure 6.7 Select 2^{23} – 1 PRBS Pattern Generator and Analyzer



Note:
If PRBS Pattern generator and analyzer is not selected, data present at the transmit 16-bit parallel bus interface will be looped-back at the received 16-bit parallel bus interface as well as transmitted at the high-speed serial interface.

Step 7. Check "**Pattern Sync**" status indicator by clicking on "**Start Poll**" button. The "**In Progress**" indicator will start flashing green when polling has begun.

Figure 6.8 Start Polling

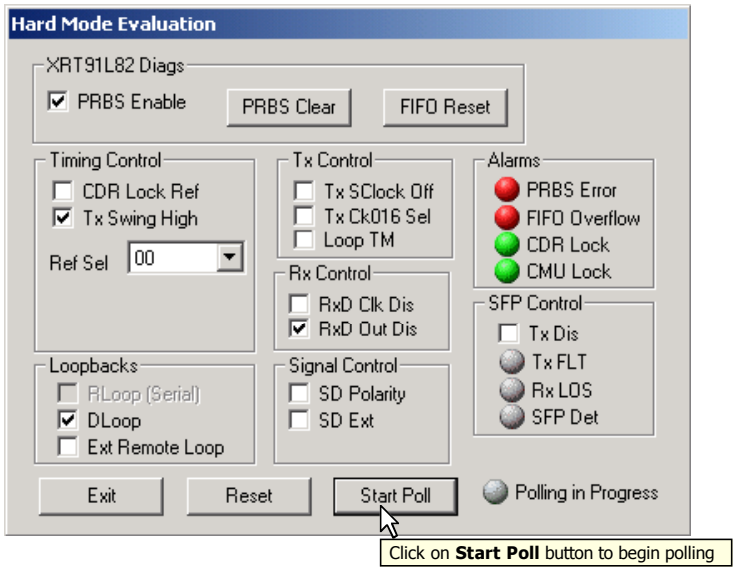
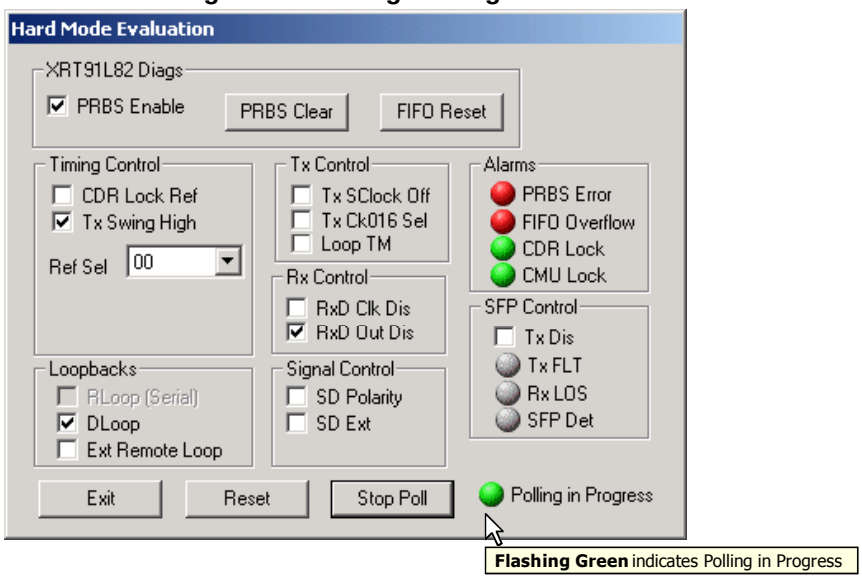
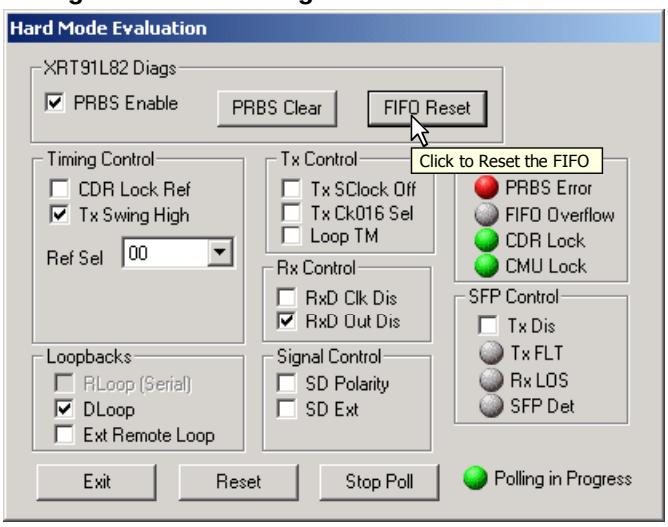


Figure 6.9 Polling in Progress



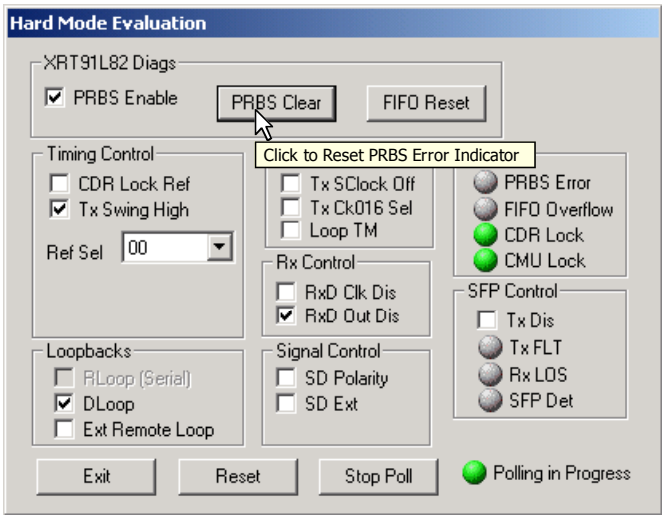
To reset the "**FIFO Overflow**" alarm indicator, click the "**FIFO Reset**" button.

Figure 6.10 Resetting FIFO Overflow Indicator



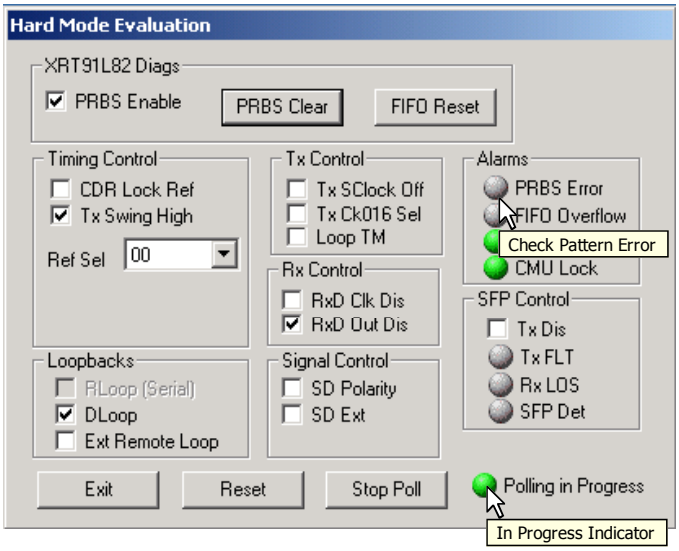
To reset the "**PRBS Error**" history indicator, click the "**PRBS Clear**" button.

Figure 6.11 Resetting PRBS Error Indicator



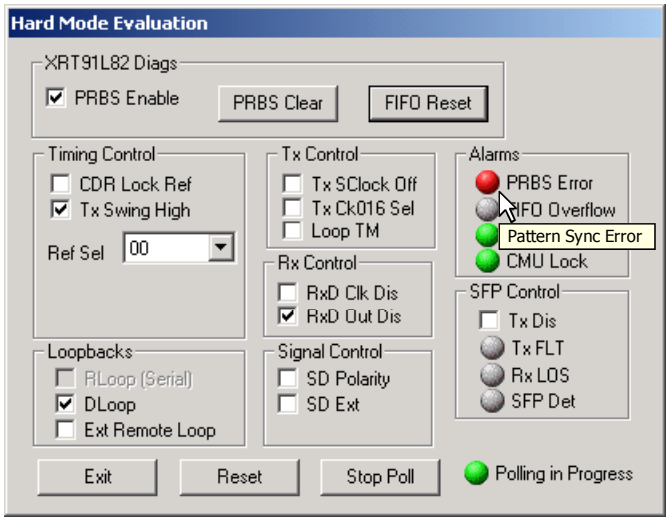
Valid PRBS pattern synchronization is indicated by a grey LED. PRBS pattern reception failure is indicated by a red LED.

Figure 6.12 Check Pattern Sync



The "**Pattern Sync Hist**" indicator flags errors in PRBS transmission and reception. Momentary and current error occurrence is indicated by a red LED.

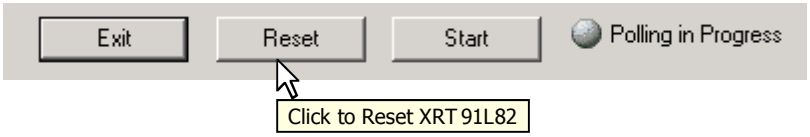
Figure 6.13 Check Pattern Loss



6.2 MASTER RESET

Whenever necessary, the XRT91L82 can be reset. To invoke this, click on the Master Reset button. This will automatically toggle the hardware reset pin on the XRT91L82.

Figure 6.14 Master Reset



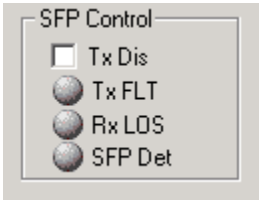
6.3 SFP MODULE CONTROL

This section is mainly a register status box that includes the ability to disable the SFP module optical transmitter.

Table 1.0 SFP Module Control Box

	Function	Description
	Tx Disable	Checking this box disables the optical transmitter
	Tx Fault	Red LED detects failure in optical transmission
	RxLOS	Red LED detects Loss of Signal
	SFP Detect	Red LED detects the absence of the SFP optical module

Figure 6.15 SFP Module Control



7.0 CONFIGURING THE XRT91L82 EVALUATION BOARD FOR JITTER MEASUREMENTS

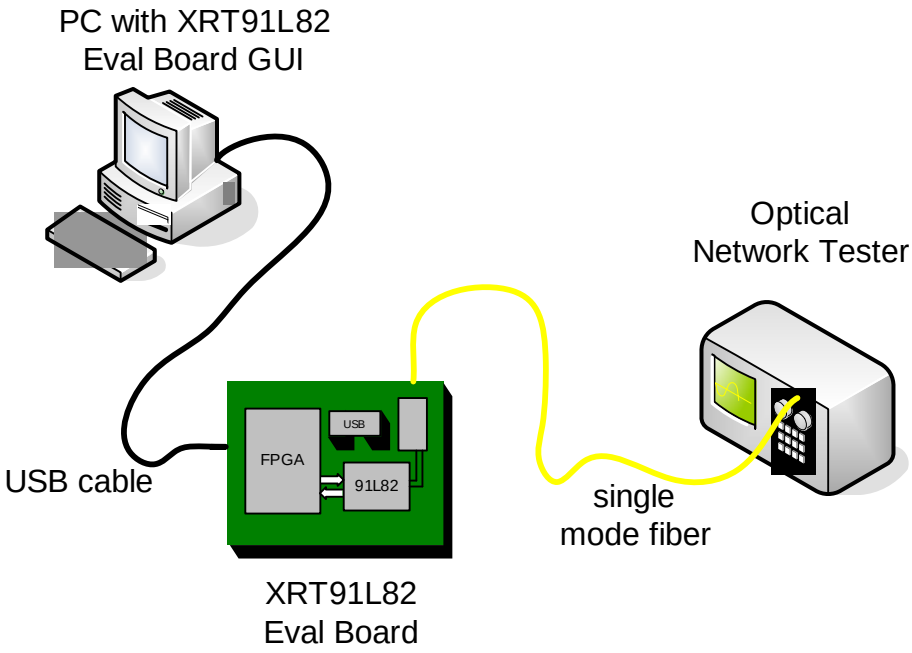
There are three types of jitter measurement of interest in the XRT91L82 transceiver product. They are received jitter tolerance, jitter transfer, and transmit intrinsic jitter.

- How to measure optical Jitter Tolerance of the XRT91L82
- How to measure optical Jitter Transfer of the XRT91L82
- How to measure optical Intrinsic Jitter of the XRT91L82

Since the XRT91L82 Evaluation Board uses an optical interface, a network tester with an optical interface capable of jitter measurements will be required to successfully characterize optical jitter performance on the XRT91L82. Below is a simple diagram of the jitter measurement setup.

To simplify the test setup, all are jitter test setup are shown using Hardware Mode on the XRT91L82. However, the user can use Host mode to perform all the jitter test and measurement.

Figure 7.0 Jitter Measurement Setup



7.1 HOW TO MEASURE OPTICAL JITTER TOLERANCE OF THE XRT91L82

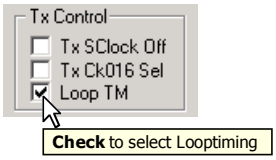
To successfully perform this test, the user needs to configure the XRT91L82 into:

- Remote Serial Loopback
- Looptiming

Step 1. Configure the XRT91L82 for Remote Serial Loopback as outlined in section 6.1.1, “Remote Serial Loopback.”

Step 2. Select **Looptiming** mode for the XRT91L82 transmit timing.

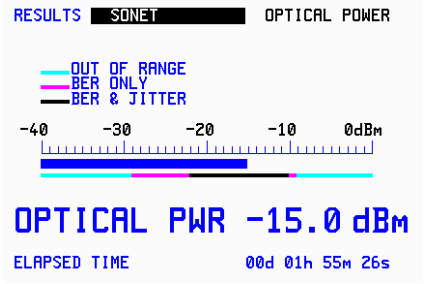
Figure 7.1 Select Looptiming



Step 3. Select the proper SONET/SDH data rate source and payload (usually 2^{23}-1 PRBS) pattern on test equipment and verify recovered data integrity and pattern sync on test equipment.

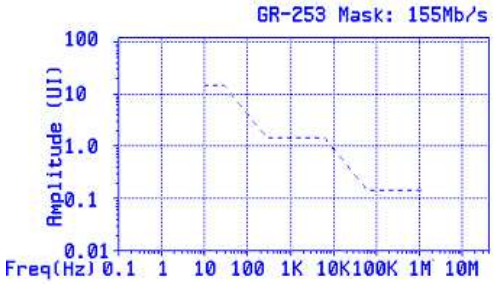
Step 4. Verify that the optical signal strength is valid for jitter measurements. Adjust optical signal strength by adding/removing optical attenuators or slightly adjusting optical coupler/connector until desired optical signal strength is achieved for valid jitter measurements.

Figure 7.2 Optical Signal Strength (Test Equipment)



Step 5. Configure the test equipment for Jitter Tolerance measurements and select the appropriate Jitter Tolerance Mask Standard for SONET STS-48/SDH STM-16.

Figure 7.3 GR.253 Jitter Tolerance Mask (Test Equipment)



Step 6. Begin Jitter Tolerance Measurements.

7.2 How to measure Optical Jitter Transfer of the XRT91L82

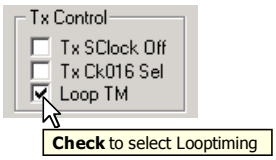
To successfully perform this test, the user needs to configure the XRT91L82 into:

- Remote Serial Loopback
- Looptiming

Step 1. Configure the XRT91L82 for Remote Serial Loopback as outlined in section 6.1.1, "Remote Serial Loopback."

Step 2. Select **Looptiming** mode for the XRT91L82 transmit timing.

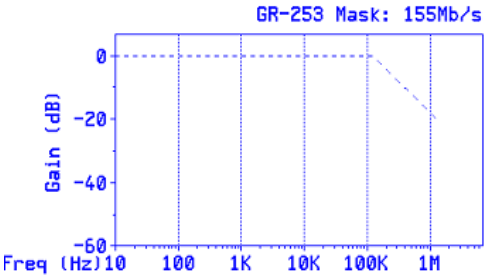
Figure 7.4 Select Looptiming



Step 3. Select the proper SONET/SDH data rate source and payload (usually 2^{23}-1 PRBS) pattern on test equipment and verify recovered data integrity and pattern sync on test equipment.

Step 4. Configure the test equipment for Jitter Transfer measurements and select the appropriate Jitter Transfer Mask Standard for SONET STS-48/SDH STM-16.

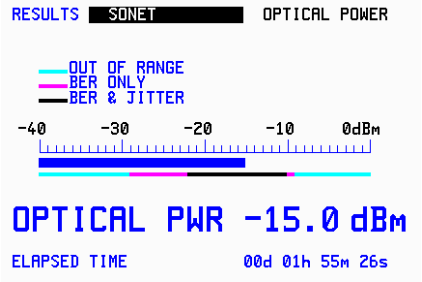
Figure 7.5 GR.253 Jitter Transfer Mask (Test Equipment)



Step 5. Most test equipment will require an initial jitter transfer calibration before proceeding with jitter transfer measurements. Therefore, detach the Evaluation Board connected optical cable from the test equipment and replace a with an optical loopback cable for the calibration process. (See Figure 7.7) Once optical loopback cable is inserted, verify data integrity and pattern sync.

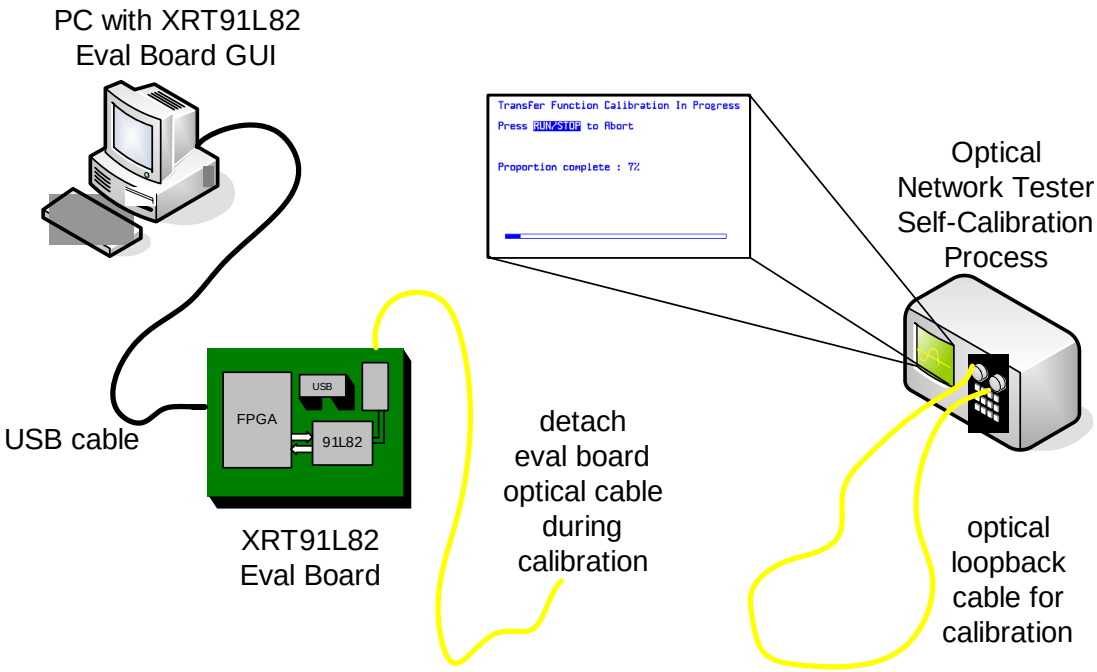
Step 6. Verify that the optical signal strength is valid for jitter measurements. Adjust optical signal strength by adding/removing optical attenuators or slightly adjusting optical coupler/connector until desired optical signal strength is achieved for valid jitter measurements.

Figure 7.6 Verify Optical Signal Strength (Test Equipment)



Step 7. Follow test equipment instructions for calibration and do not interrupt calibration process.

Figure 7.7 Jitter Transfer Calibration (Test Equipment)



Step 7. Once initial calibration is done, replace the optical loopback cable on the test equipment with the Evaluation Board optical cable. Verify that transmit and receive cables are properly oriented and test equipment receiver does not declare Loss of Signal. Once Evaluation Board optical cable is inserted and data integrity and pattern sync is achieved, verify that the optical signal strength is valid for jitter measurements before proceeding to the next step.

Figure 7.8 Reattach Evaluation Board optical cable

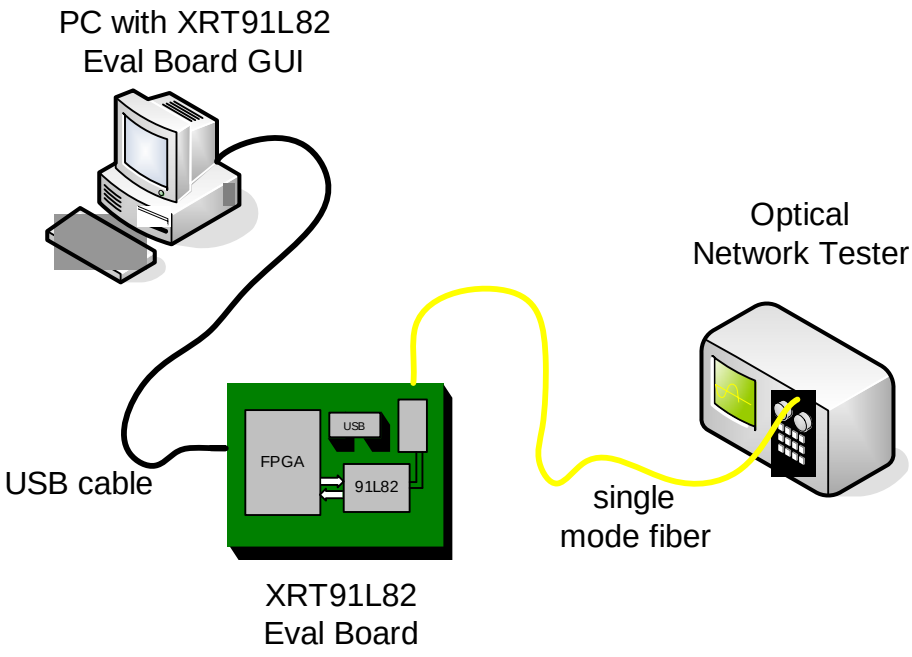
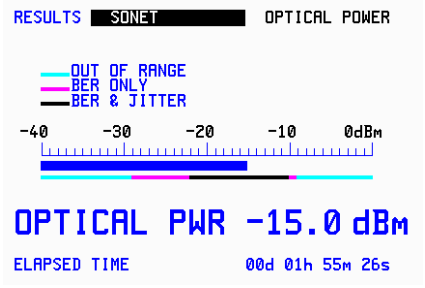


Figure 7.9 Re-Verify Optical Signal Strength (Test Equipment)



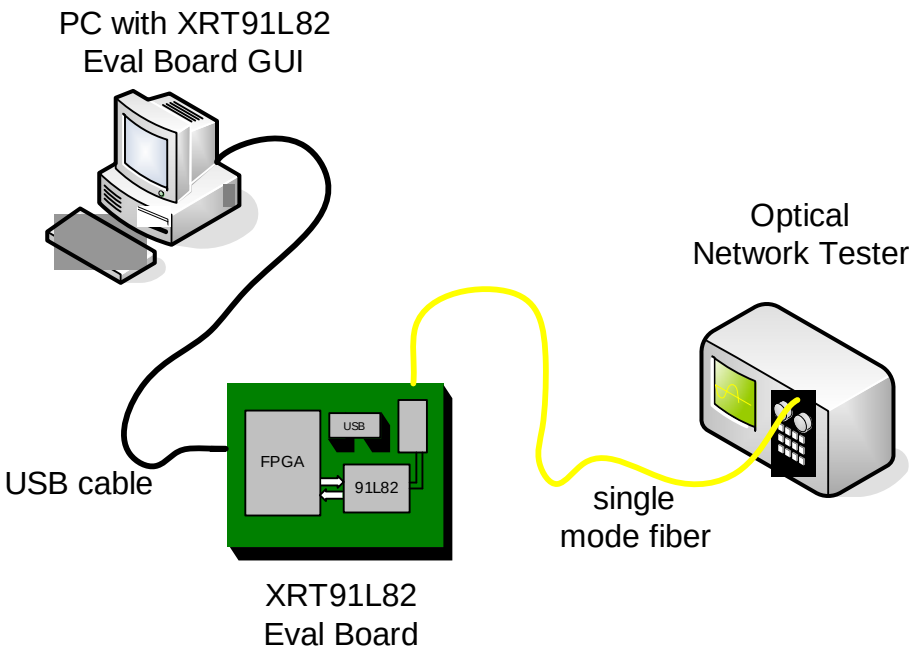
Step 8. Begin Jitter Transfer Measurements.

7.3 How to measure Optical Intrinsic Jitter of the XRT91L82

To successfully perform this test, the user needs to configure the XRT91L82 into:

- Transmit a 2^{23} -1 PRBS pattern
- Local Timing Mode

Figure 7.10 Intrinsic Jitter Measurement Test Setup



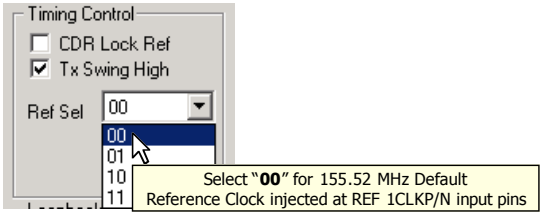
Step 1. Configure the XRT91L82 to transmit the internally generated 2^{23} -1 PRBS pattern as outlined in Example Applications in section 6.1.2, PRBS Pattern Synch Test using Digital Local Loopback. Use step 1 thru step 8.

Step 2. Remove the Digital Local Loopback. Do not enable any loopbacks.

Step 3. Select the desired reference clock frequency (155.52 MHz or 166.63 MHz) to be tested.

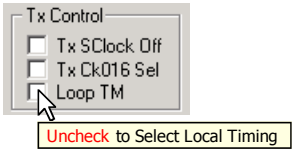
Note: All XRT91L82 boards are shipped with a standard 155.52 MHz differential reference clock oscillator. The 155.52 MHz differential clock oscillator is fed to the XRT91L82's reference clock inputs REF1CLKP/N and is installed as device **U12**. Before selecting other Reference Frequency options stated on the datasheet, **U12** and **U13** devices on the Evaluation Board must be populated with the appropriate differential clock oscillator frequencies.

Figure 7.11 Select "00" for 155.52 MHz Default Reference Clock Option



Step 4. Select **Local Timing** Mode for the XRT91L82 transmit timing.

Figure 7.12 Select Local Timing



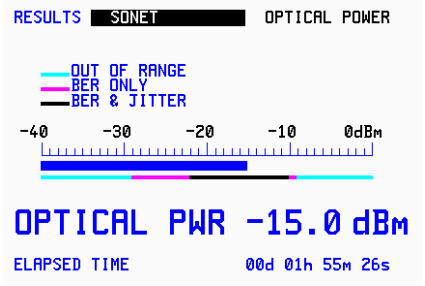
Step 4. Connect the optical cable from the OC-48/STM-16 SFP module to the Optical Network Test Equipment.

Step 5. Select the proper SONET/SDH data rate source on test equipment and verify test equipment is able to obtain valid signal from the XRT91L82 optical transmitter.

Note: Since the XRT91L82 is internally generating and independently transmitting an unframed 2^{23} -1 PRBS pattern to the SONET/SDH test equipment, data will not be recovered by the SONET/SDH test equipment. Hence, data integrity and pattern sync on the tester is **not** expected. However, tester should detect an unframed OC48/STM-16 signal.

Step 6. Verify that the optical signal strength is valid for jitter measurements. Adjust optical signal strength by adding/removing optical attenuators or slightly adjusting optical coupler until desired optical signal strength is achieved for valid jitter measurements.

Figure 7.13 Verify Optical Signal Strength (Test Equipment)



Step 7. Configure the test equipment for jitter measurements and select the appropriate SONET STS-48/ SDH STM-16 jitter frequency filters on the test equipment according to the table below.

Table 2.0 SONET/SDH Jitter Frequency Bandpass Filters (1544 kb/s Networks)

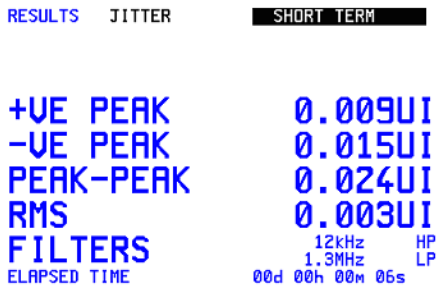
DATA RATE	SONET GR.253 FILTER STANDARD	SDH G.783 FILTER STANDARD
2488 Mbps	12 KHz – 20 MHz	12 KHz – 20 MHz

Table 2.1 SONET/SDH Jitter Frequency Bandpass Filters (2048 kb/s Networks)

DATA RATE	SONET GR.253 FILTER STANDARD	SDH G.783 FILTER STANDARD
2488 Mbps	12 KHz – 20 MHz	1 MHz – 20 MHz

Step 8. Begin measuring jitter and permit test equipment to measure peak-to-peak and rms values over a sixty-second interval (1 minute maximum) per G.783 section 9.3.1.1.

Figure 7.14 RMS Jitter Measurement (Test Equipment)



8.0 Other Measurements

The following test measurements may also be done on the XRT91L82 Evaluation Board. These types of test may require hardware board modifications.

8.1 Eye diagram test setup
8.2 XRT91L82 Current Consumption Measurement

8.1 EYE DIAGRAM TEST SETUP

To display the eye diagram pattern successfully, the user must have the following:

- A high speed digital oscilloscope
- A high impedance or 50 Ohm effective termination differential high-speed probe with a minimum bandwidth at least twice the data rate frequency (Use a probe with a minimum of 5 GHz bandwidth)
- The XRT91L82 Evaluation Board schematic for reference.

In addition, the user must configure the XRT91L82 to do the following:

- Transmit 2^{23} – 1 PRBS pattern
- Local Timing Mode

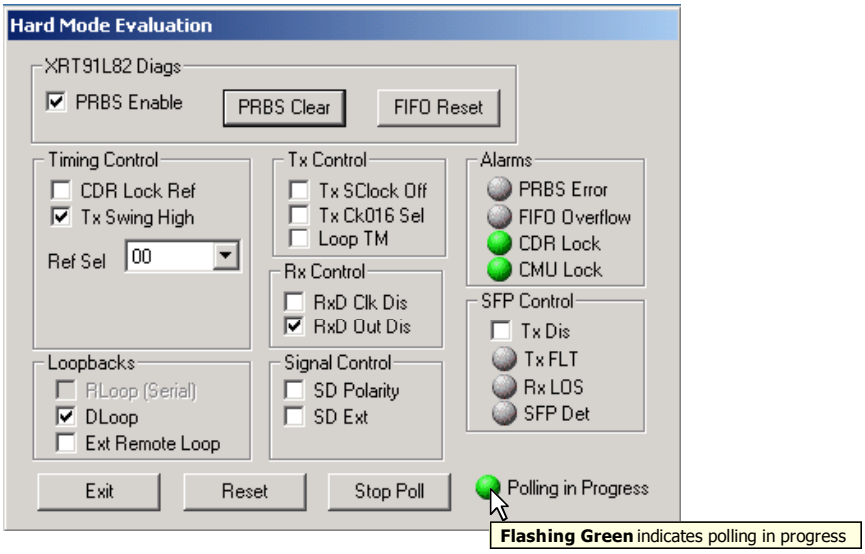
Step 1. Remove the SFP optical module. Find pin A6 and pin A5 of the XRT91L82 and trace to pins 18 and 19 of the device **U10** SFP Optical Module. These are the TXOP and TXON high speed CML differential outputs, respectively. Prepare the pins for probing, this may or may not require soldering biasing resistors as required by the differential probe manufacturer. Refer to XRT91L82 Evaluation Board schematic for reference and termination information.

Step 2. Securely and gently attach the differential high-speed probe to TXOP and TXON high speed CML differential output pins. Be extremely careful not to subject the pins to physical stress as it may be damaged. Attach the differential probe to the oscilloscope.

Step 3. Configure the XRT91L82 to transmit the internally generated 2^{23} -1 PRBS pattern as outlined in Example Applications in section 6.1.2, PRBS Pattern Synch Test using Digital Local Loopback. Use step 1 thru step 7.

Step 4. Click on "**Start Poll**" button. The "**In Progress**" indicator will start flashing green when polling has begun.

Figure 8.0 Polling in Progress



Step 5. Configure and adjust the oscilloscope settings to superimpose the XRT91L82 CML high speed differential outputs over time. Your eye diagram should look to something similar below.

Figure 8.1 XRT91L82 Eye Diagram

8.2 XRT91L82 CURRENT CONSUMPTION MEASUREMENT

To successfully measure the current consumption on the XRT91L82, the user must have the following:

- A network test equipment capable of sourcing OC-48/STM-16
- Two current meters capable of measuring current accurately in milliamps
- A voltmeter capable of measuring voltage accurately in hundredths
- The XRT91L82 Evaluation Board schematic for reference

In addition, the user may configure the XRT91L82 to do the following but is not necessary:

- FPGA Remote Loopback
- Looptiming Mode

Step 1. Review the XRT91L82 Evaluation Board schematic and locate **L2** and **L4**. These ferrite bead supplies the entire power to the XRT91L82 silicon. Note that **Vcc3v3Dut** and **Vcc1v8Dut** coming from the XRT91L82 power supply pins lead to these ferrite beads, respectively.

Step 2. Locate and remove **L2** and **L4** ferrite beads on the XRT91L82 Evaluation Board. Store **L2** and **L4** ferrite beads in a secure container for reinstallation at a later time.

Step 3. Attach and secure leads to **L2** and **L4** soldering pads. It should be long enough to prevent shorting the board. These leads should also be secured and prevented from physical stress when the current meter is attached to the leads. Attaching a 2 pin header and jumper on the free-end is useful in these applications. Check for soldering for shorts and remove errant solder on the board before proceeding. The board should be cleaned with a solder flux remover at the soldering site to prevent flux contamination and corrosion.

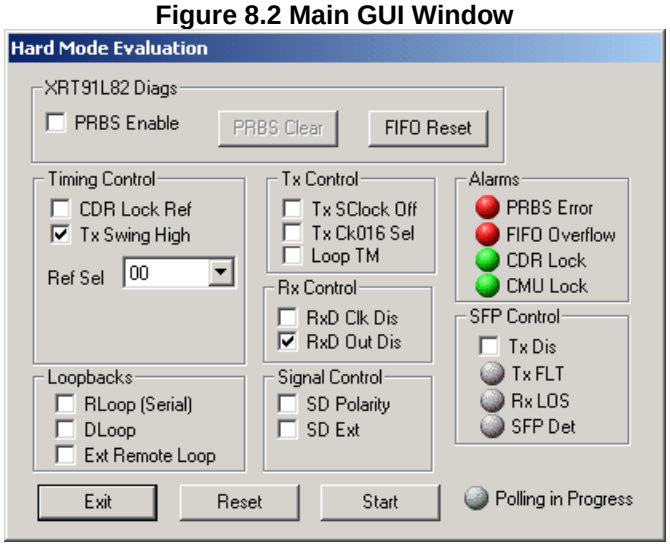
Step 4. Install the **L2** and the **L4** jumpers. Connect the USB cable to both the PC and the XRT91L82 Evaluation Board. Verify power supply on the board by checking Power LED. Remove the **L2** and **L4** jumpers. Attach the first current meter lead to the **L2 leads** and the second current meter to the **L4 leads** and verify power to the XRT91L82 by monitoring current consumption on the current meter.

Step 5. Connect the optical cable from the SFP module on the Evaluation Board to the OC-48/STM-16 Optical Network Test Equipment. This cable is included in the XRT91L82 evaluation kit. Verify optical signal strength and attached an optical attenuator to the receiver end of the test equipment if necessary.

Step 6. Launch the XRT91L82 application GUI. See section 4.1, “Starting the Evaluation Software.”

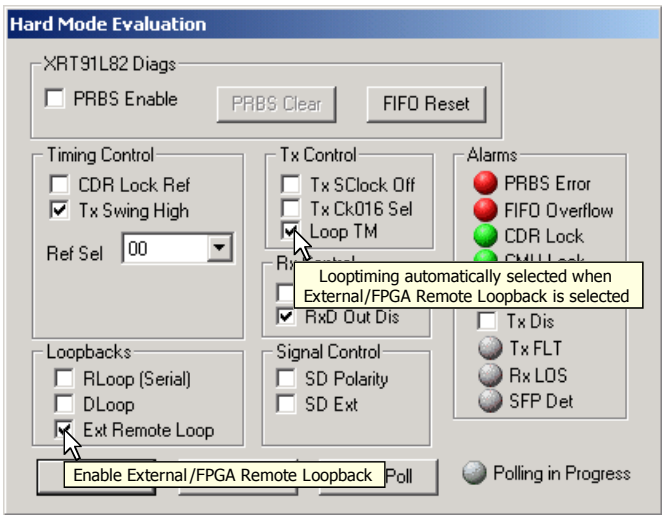
Step 7. Once the application GUI **Start Test** is running, you should see a similar window below with the XRT91L82 default settings.

Figure 8.2 Main GUI Window



Step 8. Enable the External/FPGA Remote Loopback by checking the on the "**Ext Remote Loop**" box.

Figure 8.3 Enable FPGA Remote Loopback



Step 7. Select the proper SONET/SDH data rate source and payload pattern on test equipment and verify recovered data integrity and pattern sync on test equipment. Check test equipment for valid pattern synchronization.

Note: If the test equipment receiver reports a Loss of Signal, it is likely that the optical cable is not properly oriented. Switch the transmit and receive cables on the test equipment and verify data integrity. Check the **L2** and **L4** jumper leads for proper connection as well.

Step 9. Click on "**Start Poll**" button. The "**In Progress**" indicator will start flashing green when polling has begun.

Figure 8.4 Start Polling

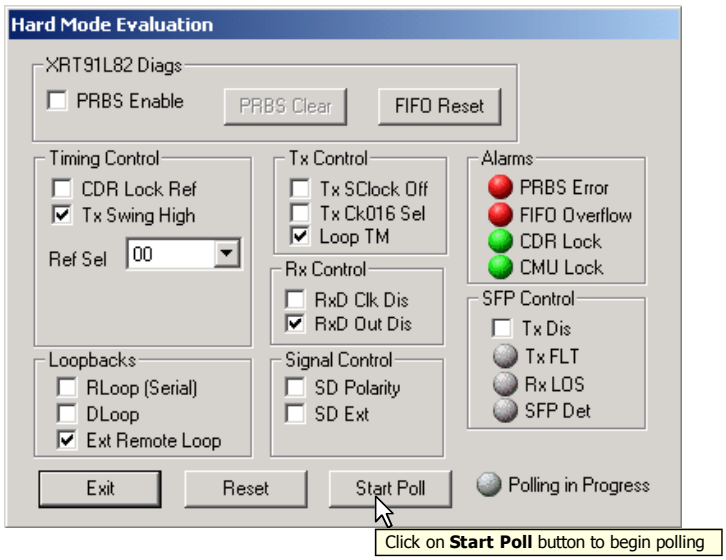
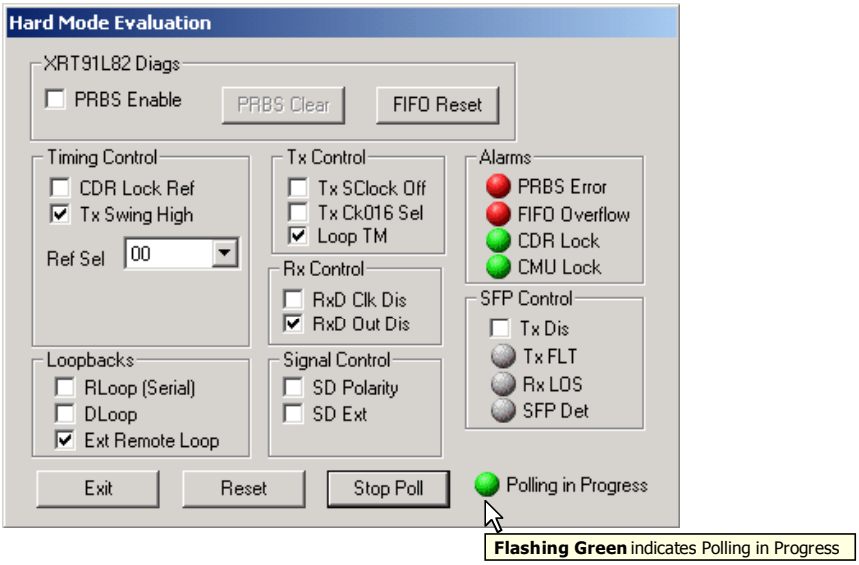
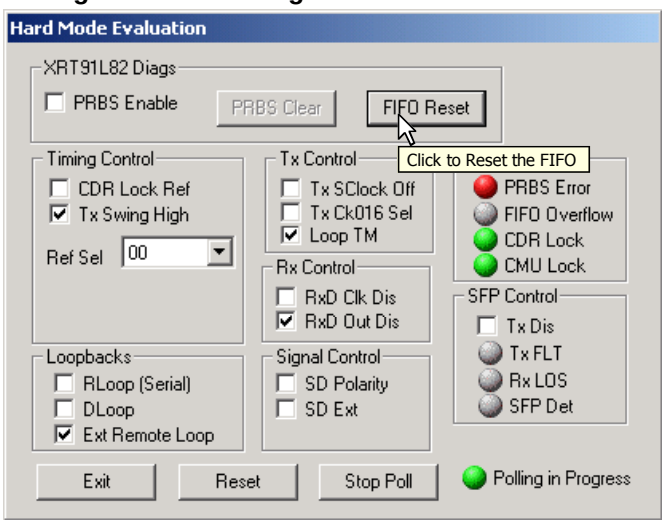


Figure 8.5 Polling in Progress



Reset the "**FIFO Overflow**" alarm indicator, click the "**FIFO Reset**" button.

Figure 8.6 Resetting FIFO Overflow Indicator



Step 11. Start the Bit-Error test on the OC-48/STM-16 Optical Network Test Equipment and check for valid pattern synchronization.

Step 12. Record the XRT91L82 current consumption and the voltage at the **L2** and **L4** pad lead with reference to board Ground, the user will need this information to calculate the total power consumption. Note that External/FPGA Remote Loopback exercises all the logical blocks and analog drivers in the XRT91L82 thereby providing the worst-case condition for power consumption measurement.